

S/N 10/052952

PATENT

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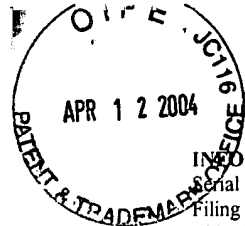
Applicant:	Leonard Forbes et al.	Examiner:	Jerry T Rahl
Serial No.:	10/052952	Group Art Unit:	2874
Filed:	January 17, 2002	Docket:	1303.034US1
Title:	THREE-DIMENSIONAL PHOTONIC CRYSTAL WAVEGUIDE STRUCTURE AND METHOD		

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 19-0743 in order to have this Information Disclosure Statement considered.



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The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

LEONARD FORBES ET AL.

By their Representatives,

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4/8/04

By

Viet V. Tong
Reg. No. 45,416

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 8th day of April, 2004.

Name

Amy Moriarty

Signature



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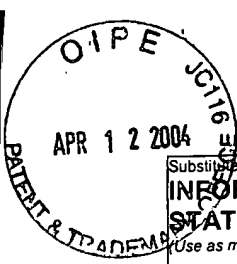
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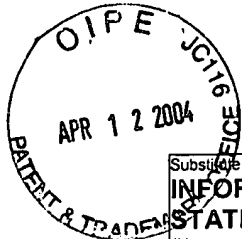
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Group Art Unit	2874
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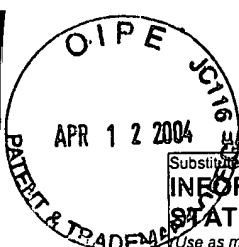
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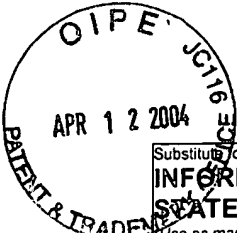
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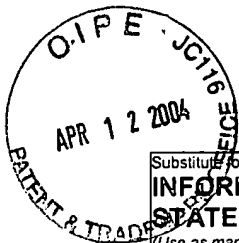


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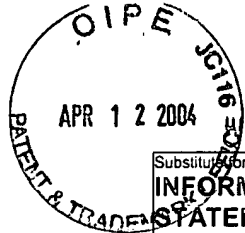
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Application Number	10/052952
Filing Date	January 17, 2002
First Named Inventor	Forbes, Leonard
Group Art Unit	2874
Examiner Name	Rahll, Jerry

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OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
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		YIN, HAIZHOU , "High Ge-Content Relaxed Sil-xGex Layers by Relaxation on Complaint Substrate with Controlled Oxidation", <u>Electronic Materials Conference, Santa Barbara, June 2002, (June 2002),8</u>	
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